EFOP-3.4.3-16-2016-00009

A felsőfokú oktatás minőségének és hozzáférhetőségének együttes javítása a Pannon Egyetemen

FPGA-BASED EMBEDDED SYSTEM DEVELOPMENT

(VEMIVIB334BR)

Created by Zsolt Voroshazi, PhD

voroshazi.zsolt@mik.uni-pannon.hu

Updated: 13. Feb. 2024.

SZÉCHENYI 2020

MAGYARORSZÁG KORMÁNYA

Európai Unió
Európai Strukturális és Beruházási Alapok

BEFEKTETÉS A JÖVŐBE

2. FPGAS & PLATFORMS

Embedded Systems

SZÉCHENYI 2020

MAGYARORSZÁG KORMÁNYA

Európai Unió
Európai Strukturális
és Beruházási Alapok

BEFEKTETÉS A JÖVŐBE

Topics covered

1. Introduction – Embedded Systems
2. **FPGAs, Digilent ZyBo development platform**
3. Embedded System - Firmware development environment (Xilinx Vivado – „EDK” Embedded Development)
4. Embedded System - Software development environment (Xilinx VITIS – „SDK”)
5. Embedded Base System Build (and Board Bring-Up)
6. Adding Peripherals (from IP database) to BSB
7. Adding Custom (=own) Peripherals to BSB
8. Development, testing and debugging of software applications – Xilinx VITIS (SDK)
9. Design and Development of Complex IP cores and applications (e.g. camera/video/ audio controllers)
10. HW-SW co-simulation and testing(Xilinx Vivado ChipScope)
11. Embedded Operation System I.: Application development, testing, device drivers, and booting
12. Embedded Operation System II.: setting and starting Linux system on ARM/MicroBlaze processor

PLD & FPGA CIRCUITS

General description

SZÉCHENYI 2020

MAGYARORSZÁG KORMÁNYA

Európai Unió
Európai Strukturális
és Beruházási Alapok

BEFEKTETÉS A JÖVŐBE

PAST …

- Before ’80s, designing logic networks for digital circuits, modern development tools were not yet available as today.
- The design of high complexity (multi I/O) logical combination and sequential networks was therefore slow and cumbersome, often coupled with paper-based design, multiple manual checks, and calculations.
- We could not talk about advanced design and simulation tools (**CAD**) either, so there was a high probability of error in a prototype design.

… AND PRESENT

- Today, all of these are available in an automated way (**EDA - Electronic Design Automation**), which, in addition to the use of **Programmable Logic Devices** (**PLD**), is relatively fast for both **Printed Circuit Boards** (**PCB**) and **Application-specific Integrated Circuits and Processors (ASIC** / ASSP).
- EDA now supports prototype development-, implementation-, and testing (verification), and it minimizes any errors that may occur.
- *Hardware / firmware / software* components can be designed and tested together (cooperatively) and in a consistent manner.

PLD and ASIC

- *Automated electronic design (**EDA**),* the use of *programmable logic devices (**PLDs**)* further reduces development time and thus minimizes costs.
- In many application areas, it is better to first implement and test the development of a given function on a programmable logic device, and then, if the conditions specified in the requirement specification are met, only the *application-specific integrated circuit* (**ASIC**) corresponding to the tested function can be designed, manufactured and tested.
- This can greatly shorten the development time of ASIC circuits and reduce *non-return costs (NRI).*

Programmable Logic Devices

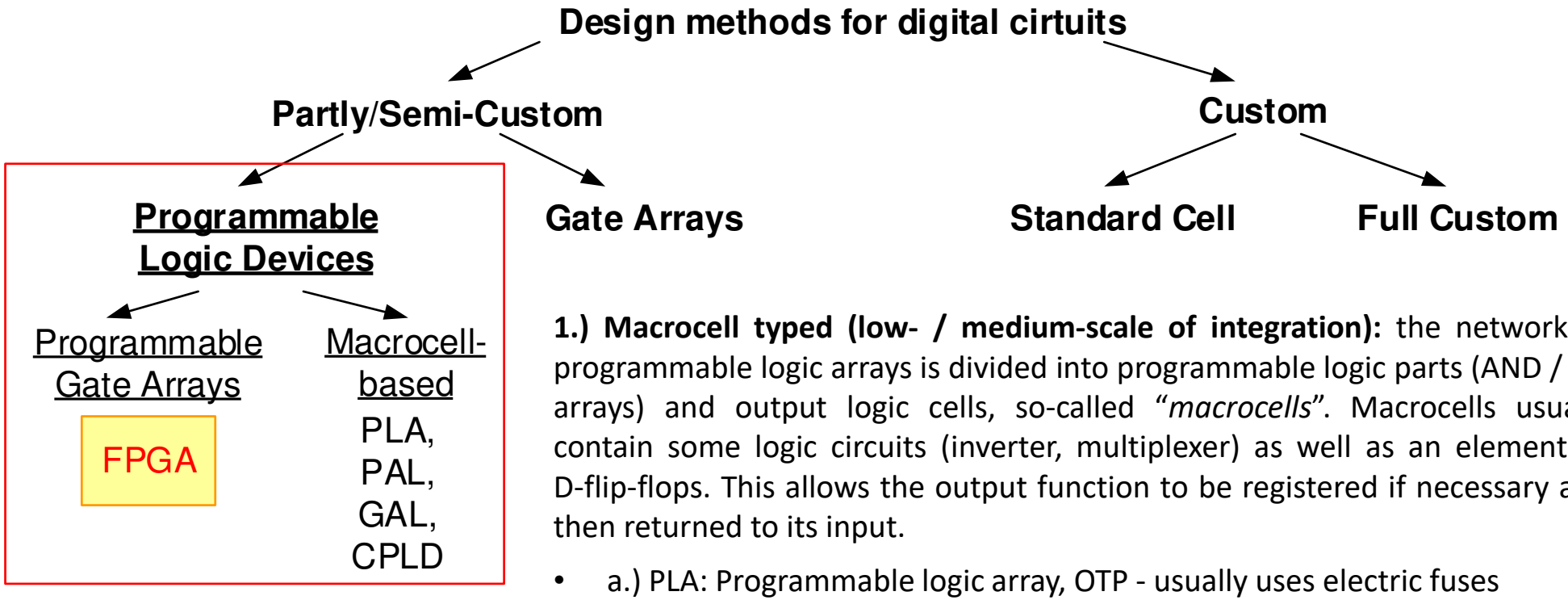
- PLDs can generally be used to design combinational logic networks and sequential networks. However, while traditional combinational logic networks have dedicated connections or a fixed function (output function), in case of PLDs exactly these can be changed in the following possible ways:
  - *1. User-programmable / configurable logic devices* (**OTP**: **One Time Programmable**), in which a function not defined during production can be changed only once (such as early fuse-based PAL, PLA devices)
  - 2. Logical devices that can be programmed several/multiple times, even in any way = ***REconfigurable*** (such as the previous GAL or today's modern CPLDs, FPGAs)

Configuration = „Programming” techniques

Configuration - "program" the device by the help of a special (now usually JTAG standard) programmer, i.e. you have to download the configuration file (bit file or object file). For most PLDs, programming is done by setting them depending on the physical type of the internal programmable connections. The following possible components are included in the programmable connections as switching elements:

- **Fuse**: After „melting”, the programming process (OTP) cannot be reversed. Previously used as a popular switch element for PAL devices,
- **Antifuse technology**: (OTP), after ‘melting down’ the antifuse crystal structured switching element, a very stable connection is obtained, which unfortunately is a non-reversible process. The technology is expensive due to the large number of mask layers required for its manufacturing, but its interference protection is very good (e.g. in space exploration),
- **SRAM cell + transistor**: arbitrarily programmable (the most common switching technology for FPGAs), the gate electrode of the transistor can be controlled depending on the initialization value stored in the SRAM,
- **SRAM cell + multiplexer**: arbitrarily programmable, depending on the value stored in the SRAM cell (selector signal) the multiplexer can be controlled,
- **Floating Gate technology**: electrically programmable, based on today's EEPROM / Flash technology.

Design methods



1.) Macrocell typed (low- / medium-scale of integration): the network of programmable logic arrays is divided into programmable logic parts (AND / OR arrays) and output logic cells, so-called "*macrocells*". Macrocells usually contain some logic circuits (inverter, multiplexer) as well as an elementary D-flip-flops. This allows the output function to be registered if necessary and then returned to its input.

- a.) PLA: Programmable logic array, OTP - usually uses electric fuses
- b.) PAL: Programmable AND / array logic, OTP - usually uses electric fuses
- c.) GAL: Generic array logic: improvement of PAL, but can be erased and programmed several times (high degree of integrity):
- d.) CPLD: Complex Programmable Logic Device

2.) Programmable gate circuits (very high-scale of integration):

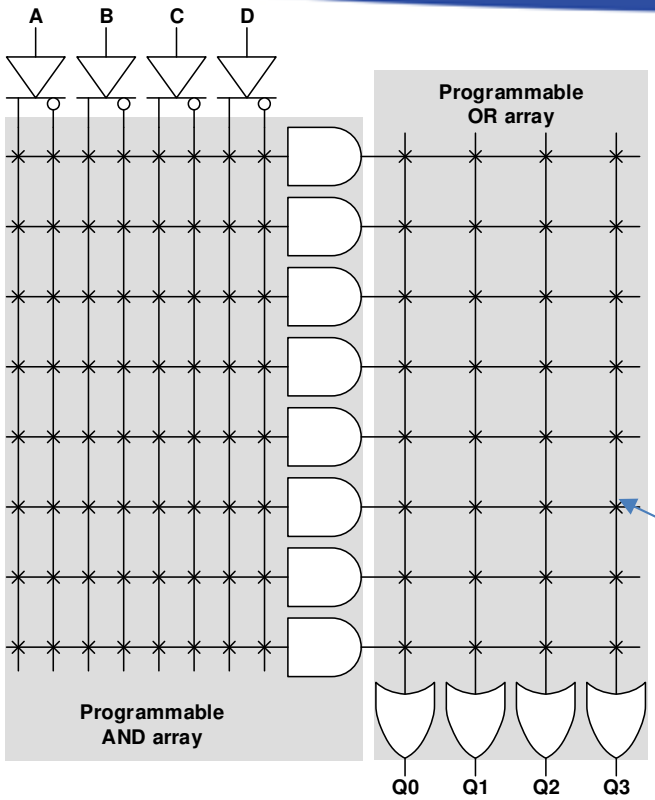
- FPGA: User Programmable (=reconfigurable) Gate Arrays

Main types of PLDs

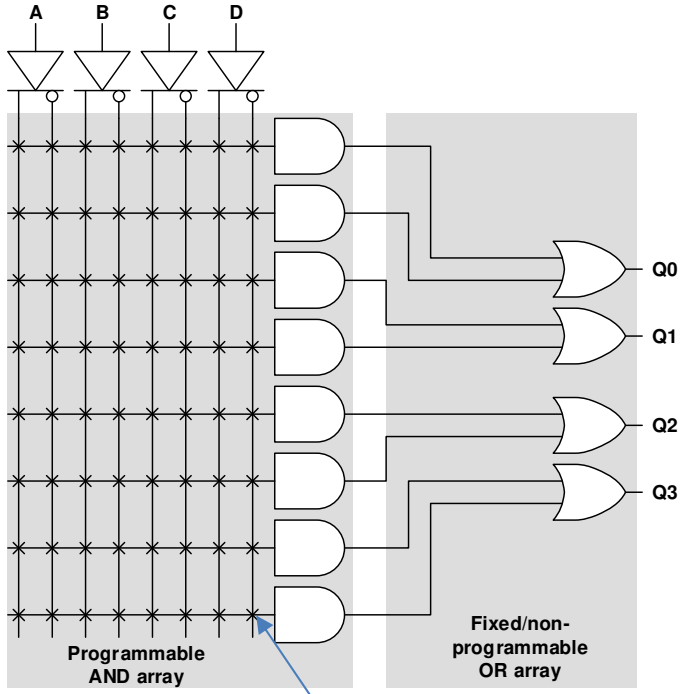
- **1.) Macrocell-based PLDs**
  - PLAs, PALs, GALs (deprecated)
  - **CPLDs**
- **2.) FPGAs (Field Programmable Gate Arrays):** **”Felhasználó által programozható/újrakonfigurálható kapuáramkörök” – in hungarian**
  - **AMD-XILINX** (Spartan, Virtex, Kintex, Artix) **~ 49% !**
  - **Intel-FPGA** (Agilex, Stratix, Arria, Cyclone)~ 40%
  - Lattice 6%
  - MicroChip (MicroSemi/Actel) ~4%
  - QuickLogic & other smaller vendors <1%

Macrocell-based PLDs

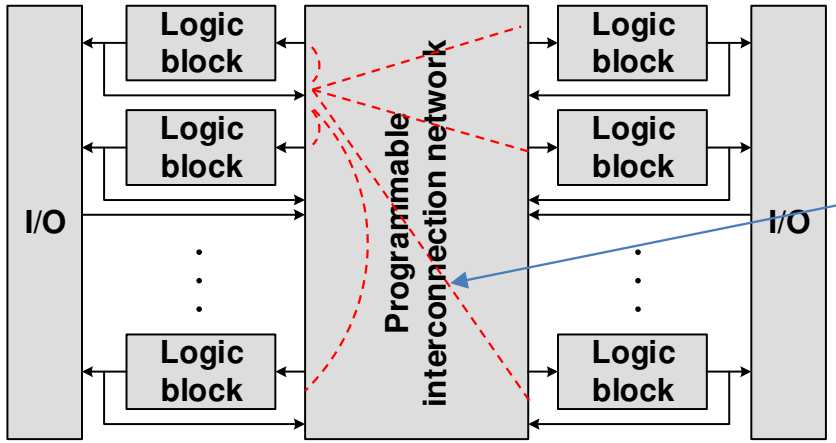
PLA

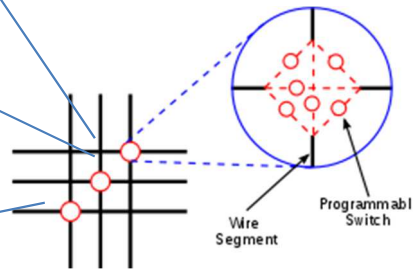


PAL



CPLD

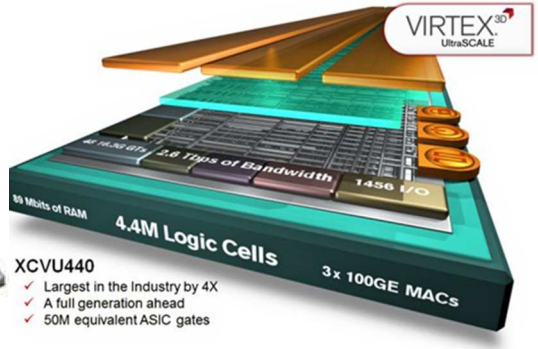


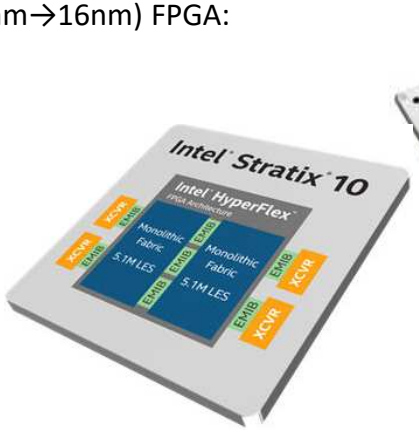


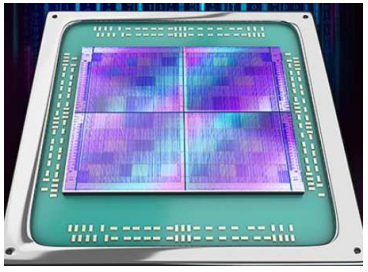
FPGA

Field **P**rogrammable **G**ate **A**rrays = architecturally reflects PALs/CPLDs, but outperforms the complexity of CPLDs. They have large/very large scale of integrity containing ~10.000 - ~100.000.000 *equivalent logic gates* depending on vendor and device type (part).

- *Equivalent transistor count#*
  - Xilinx Virtex-7 2000T #6.5 billion tr. (2012 – 28nm), equal with ~2 million logic cells.
  - Xilinx Virtex-Ultrascale+ XCVU440 (2015 – 20nm→16nm) FPGA:
    #20 billion tr. - ~**4.4** million logic cells!
    (equal with ~ 50 million logic gates)
  - Intel/Altera Stratix-10, **#30 billion trans**.
    (2016, **5.5** million logic cells,
    4-core ARM-Cortex A53, 14nm)
  - Xilinx Virtex Ultrascale+ VU19P,
    #35 billion trans., 16 nm
    (2019, ~**9** million logic cells)
  - Intel Strarix-10 GX 10M, #43.3 billion trans., 14 nm
    (2020**, 10.2** million logic cells), Dual FPGA cores!
  - Xilinx Versal ACAP, #50 billion trans. 7nm.
    (2020, 7.4 million logic cells)
  - Xilinx Versal ACAP
    50 billion trans. 7nm.
    (2020, **7.4** million logic cells)
  - AMD Versal VP1902 SoC
    (2024?, **18.5** million logic cells)
    Quad FPGA cores!

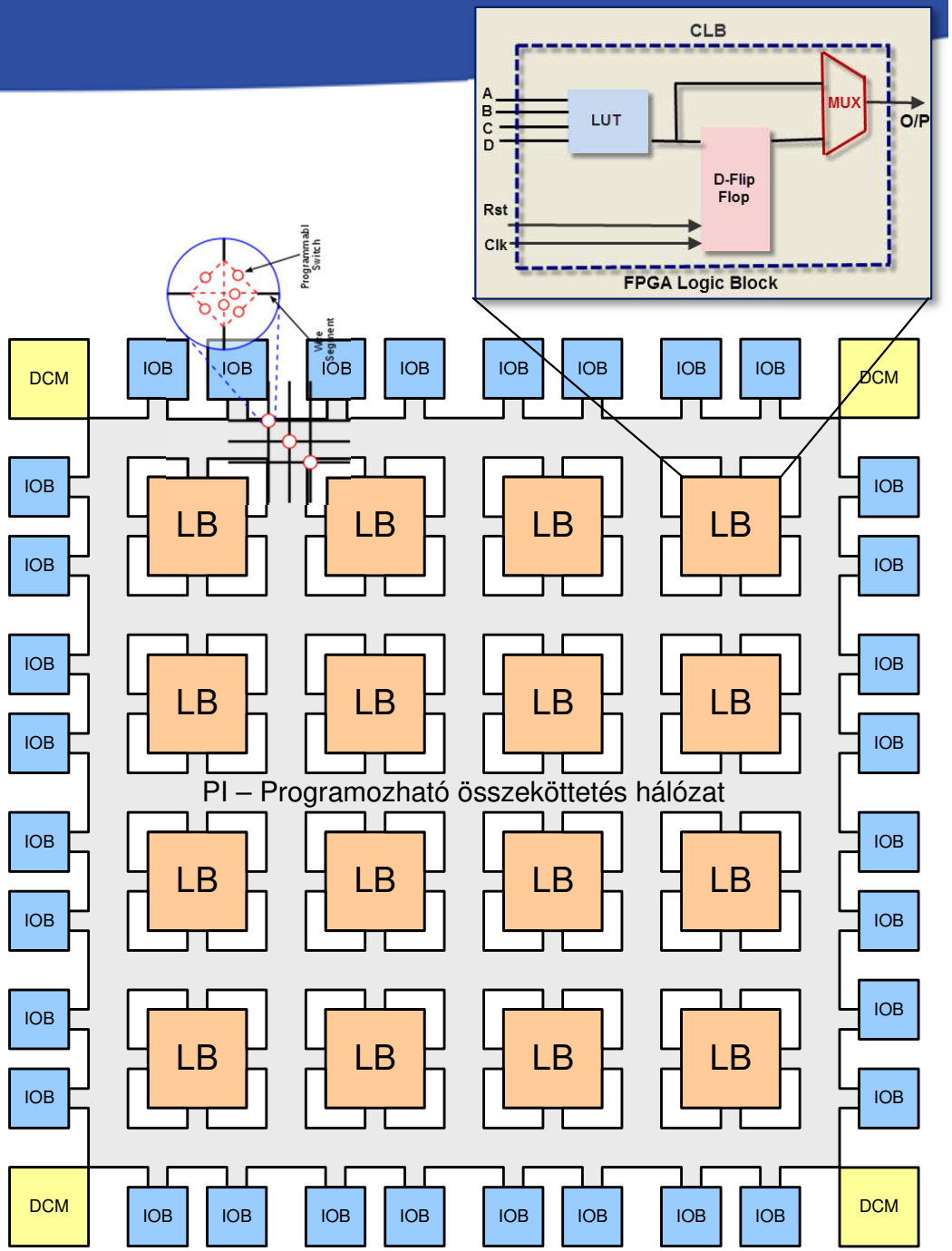






FPGA – „general” resources

- **LB / CLB**: **Configurable Logic Blocks** in which LUTs (Look-up-tables) can be used to implement any multi-input (4 or 6) single-output logic functions. These output values can be stored in a D flip-flop, if necessary; they also include multiplexers, simple logic gates, and connections.
- **IOB: I/O Blocks** that connect the internal programmable logic to the outside world. They support 30 industry standards (e.g. LVDS, LVCMOS, LVTTL, SSTL, etc.).
- **PI: Programmable Interconnection** network connects the internal components of the FPGA (using local, global, and regional routes configured by configurable switches)
- **DCM/PLL: Digital clock management** circuit capable of generating internal clock (s) with any phase and frequency from an external reference clock.



FPGA – „dedicated" resources

„Dedicated" resources which can vary greatly depending on FPGA device and complexity:

- **BRAM**: single-/dual-ported Block-RAM memories can store large amounts (×100Kbyte - upto ×10Mbyte) of data / instructions, each with a capacity of 18K / 36 Kbit)
- **MULT / DSP** Blocks: embedded multiplier circuits that can be used to perform conventional multiplication operations or even more complex DSP MAC (multiplication-accumulation) as well as arithmetic (subtraction) and logic operations at high speed.
- **Embedded processor (s):**
  - Arbitrarily configurable / **embeddable** so-called „soft" processor core(s)
    - E.g: Xilinx PicoBlaze, Xilinx MicroBlaze, Altera Nios II, ARM-Cortex-M0-3, etc.
  - Fixed **embedded**, so-called „hard" processor core(s) = silicon device
    - E.g: IBM PowerPC 405/450 (Xilinx Virtex 2 Pro, Virtex-4 FXT, Virtex-5 FXT), ARM Cortex-A9/A53/A72 (Xilinx Zynq or Altera Cyclone V SoC, Arria V SoC, or MicroSemi Smartfusion-1, - 2 FPGA chips) etc.

FPGA - Pros & Contras?

Today's modern FPGA-CPLD has

- high degree of flexibility,
- high computing power,
- relatively rapid prototyping development – thereby,
- low cost of production (time to market).

- These advantages all provide a very good alternative to microcontroller (MCU) and DSP-based implementations (e.g. in signal processing, network encryption, embedded systems, etc. applications). The long design time of an ASIC can be accelerated by FPGA-based prototyping designs.
- FPGA development is well reflected in the high degree of similarity between the improvements of microprocessors and FPGA circuit technology in terms of *scaling-down* - according to *Gordon Moore's Law*.
- Today, FPGAs contain more transistors than their modern CPU-MPU-GPU rivals (~50 billion).

EMBEDDED PROCESSORS OF XILINX FPGA

Xilinx Zynq-7010

SZÉCHENYI 2020

MAGYARORSZÁG KORMÁNYA

Európai Unió
Európai Strukturális
és Beruházási Alapok

BEFEKTETÉS A JÖVŐBE

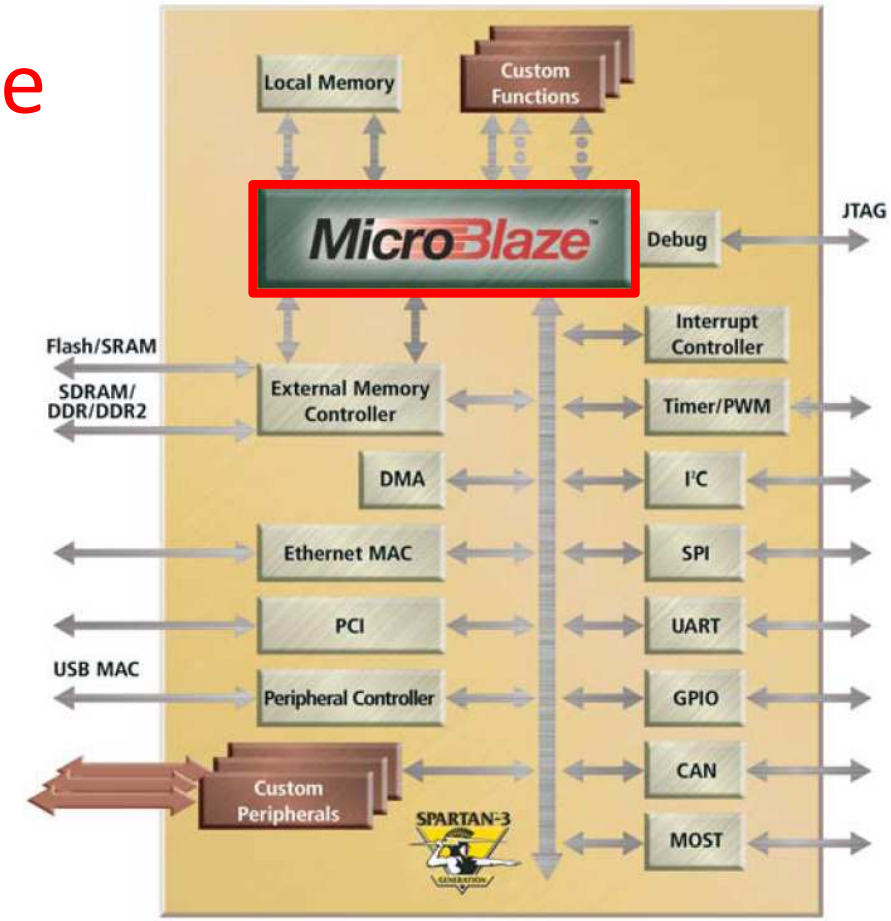
Embedded processor types

- **"Embeddable" soft-processor cores:**
  - Xilinx PicoBlaze: 8-bit (based on VHDL, Verilog HDL sources)
  - Xilinx MicroBlaze: 32-bit (VITIS / Vivado / XPS* = EDK + SDK support!)
    - Can also be connected to the PLB, OPB buses (*deprecated), **AXI bus** interfaces
  - 3rd Party: Non-Xilinx Manufacturers Processors (HDL)
    - ARM Cortex-M1 / Cortex-M3: 32 bit (licensed cores)
- **"Embedded" hard-processor cores:**
  - IBM PowerPC 405/450 processor (dedicated): 32-bit (EDK / SDK support), integrates with PLB bus system
    - but only on old Virtex II Pro, Virtex-4 FX, Virtex-5 FXT FPGAs!
  - ARM Cortex-A series processors (dedicated): Can be integrated directly into the ARM AMBA-AXI bus interface
    - ARM Cortex A9 cores (32-bit) integrated on Xilinx Zynq **APSoC**
    - Xilinx UltraScale MPSoC integrated ARM A53 / A72 cores (64-bit)
    - Intel Stratix-10 integrated ARM Cortex A53 cores (64-bit) , etc.

MicroBlaze – soft processor core

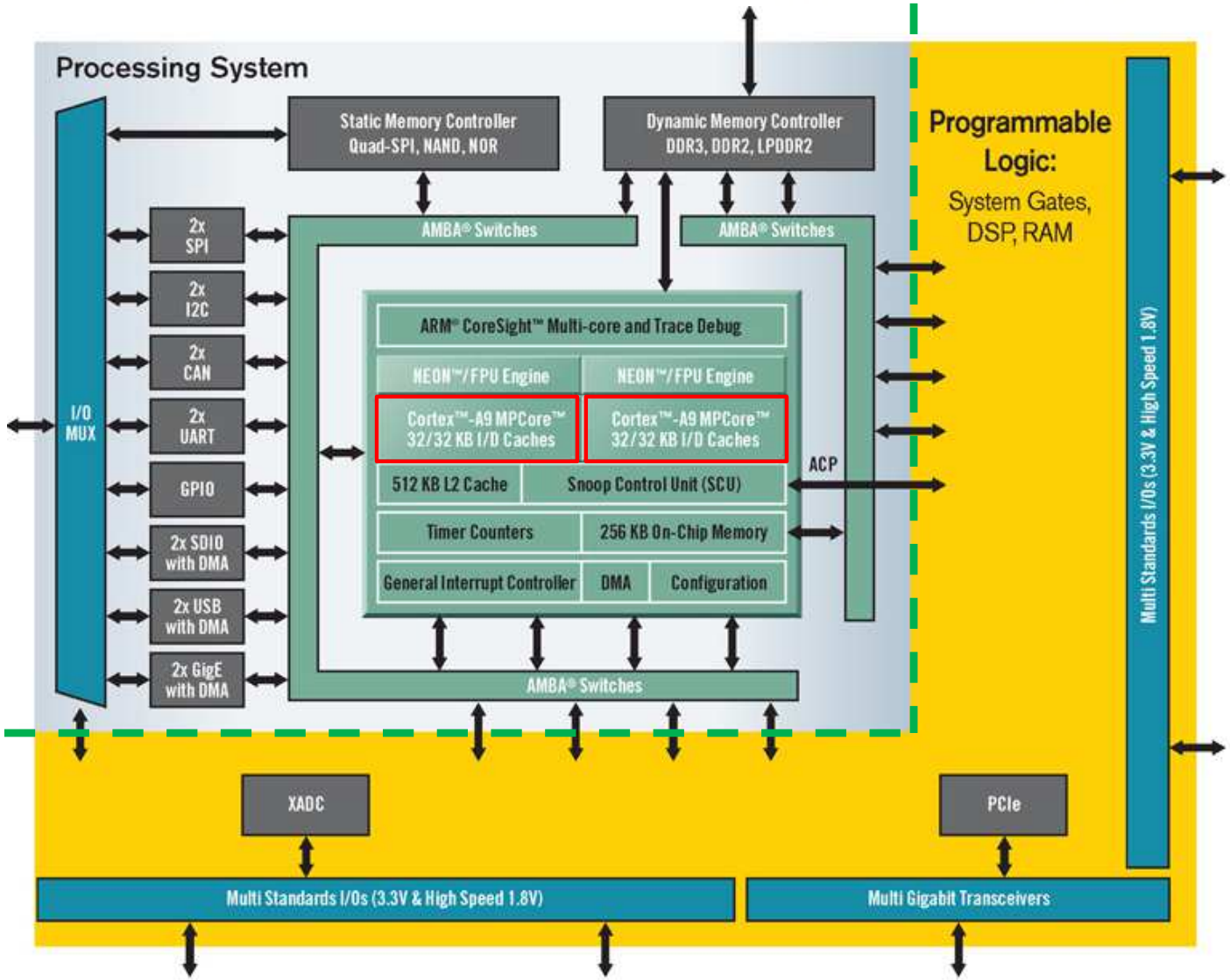
"Embeddable" processor core

- **RISC instruction set architecture**
- **32-bit soft processor core**
- **133+ MHz clock signal (PLB* / AXI bus)**
- **Harward memory architecture**
  - Instruction Cache / Data Cache
- Low power consumption: ~ mW / MHz
- 3-/5-stages of data line pipe-line
- #32 of 32-bit general purpose registers
- Timing options (timer/counter)



- Many peripherals, communication interfaces can be connected (IP cores)
- It can be implemented on **any** Xilinx FPGA that has sufficient programmable logic resources and is supported by the development software!

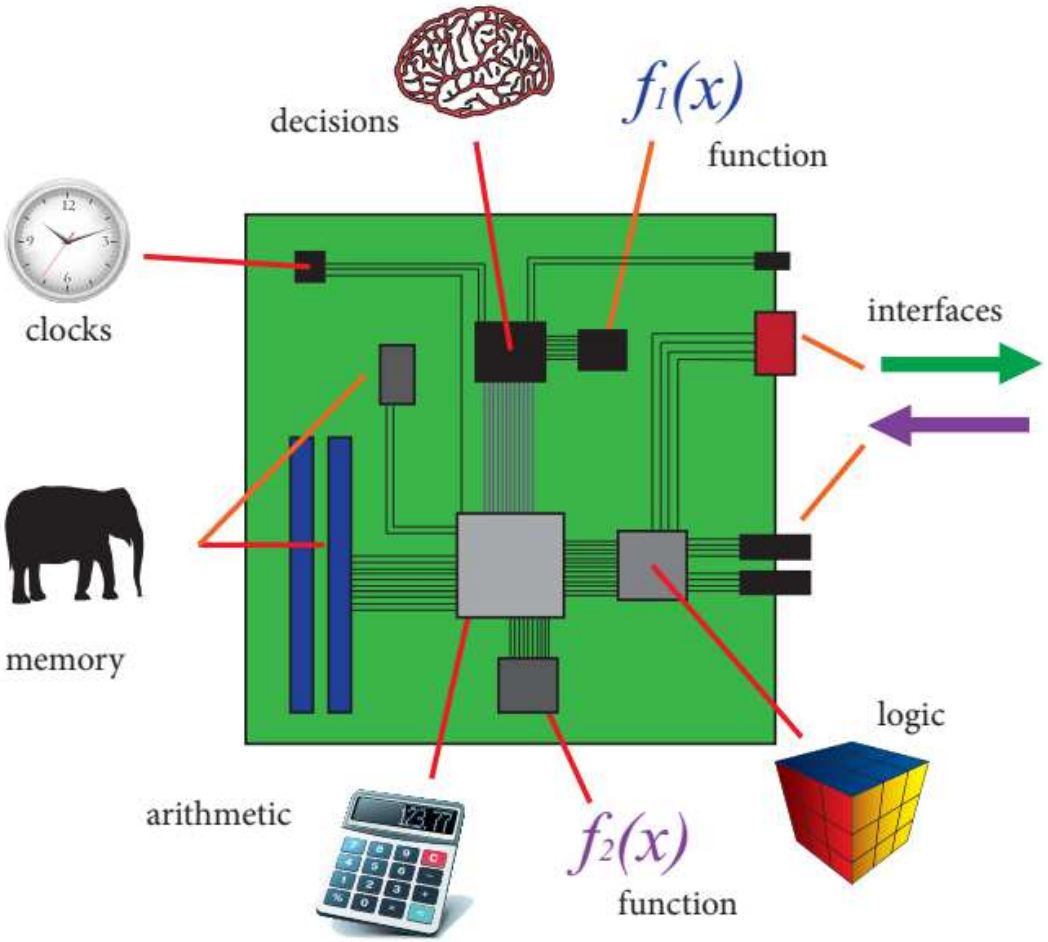
Xilinx Zynq APSoC – ARM hard-processor



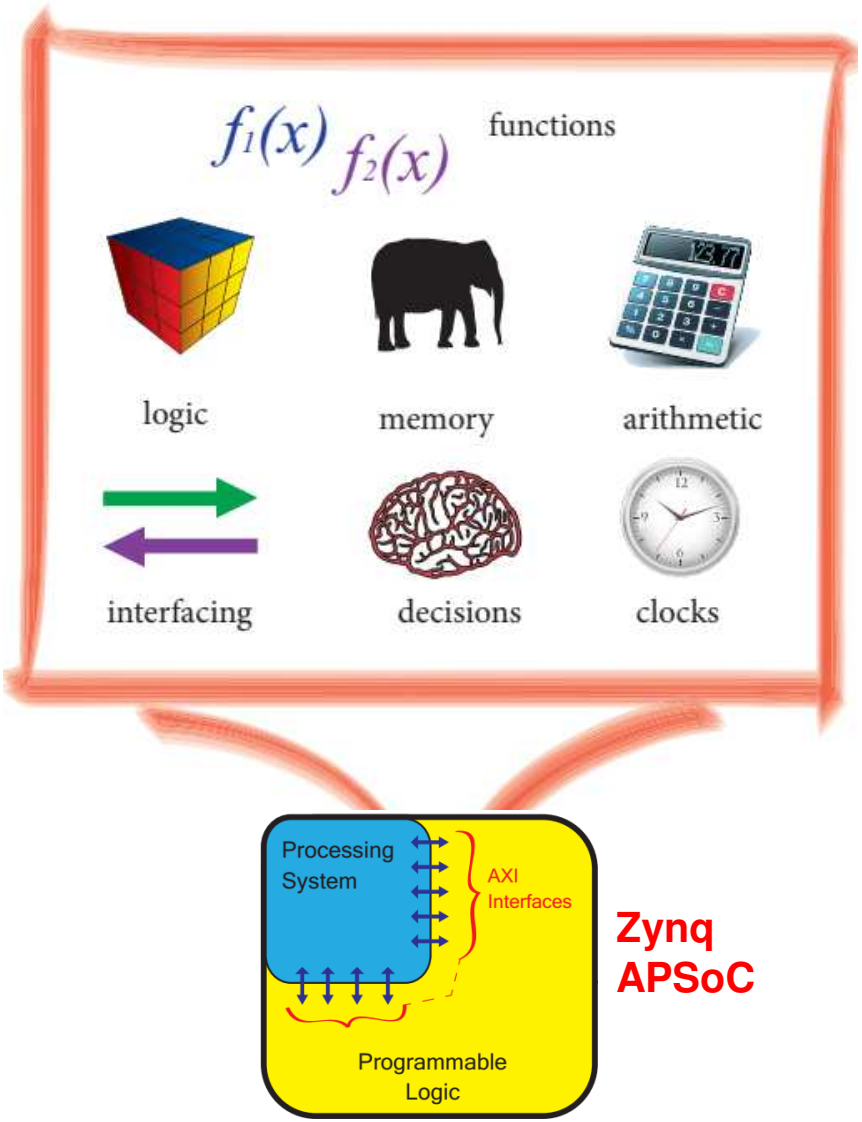
APSoC = All Programmable System-On-a-Chip

- **Dual ARM Cortex™-A9 embedded proc: 650MHz - ZYBO)**
- Neon: 32- / 64-bit FPU
- 32kB instruction & 32kB data L1 Cache
- Shared 512kB L2 Cache
- 256kB on-chip memory
- Integrated DDR3 controller
- Integrated QSPI, NAND/NOR Flash memory controller
- Peripherals: 2x USB2.0 (OTG), 2x GbE, 2x CAN2.0B 2x SD / SDIO, 2x UART, 2x SPI, 2x I2C, 4x 32b GPIO, Two 12-bit 1Msps ADCs
- 28nm Programmable FPGA Logic:
- 28k - 350k Logic Cell (~ 430k to 5.2M equivalent gate)
- 240KB - 2180KB Block RAM
- 80 - 900 18x25 DSP multiplier (58 - 1080 GMACS -DSP performance)

RECALL: System-On-a-Board vs. System-On-a-Chip



vs.



FPGA DEVICE

Xilinx Zynq-7010 APSoC

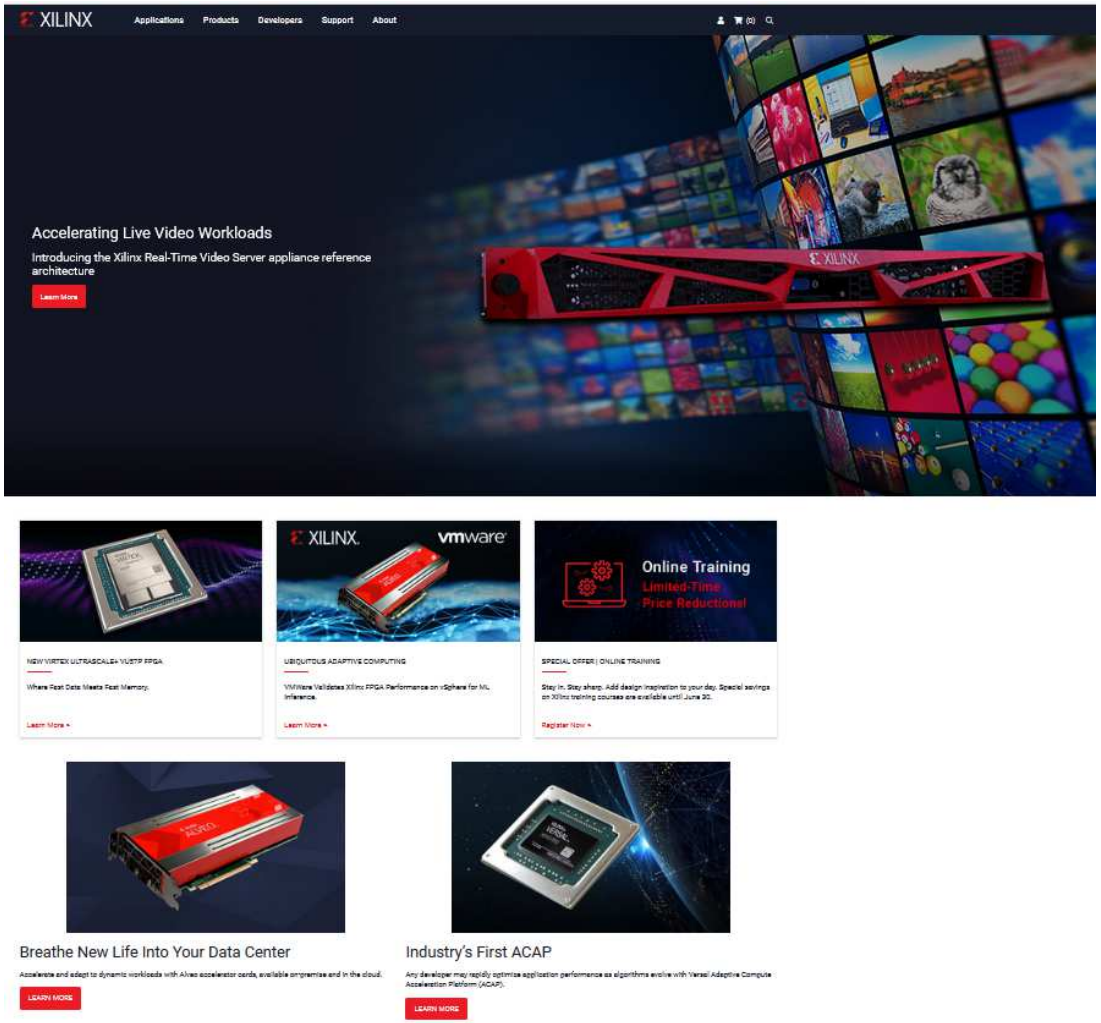
MAGYARORSZÁG KORMÁNYA

Európai Unió
Európai Strukturális
és Beruházási Alapok

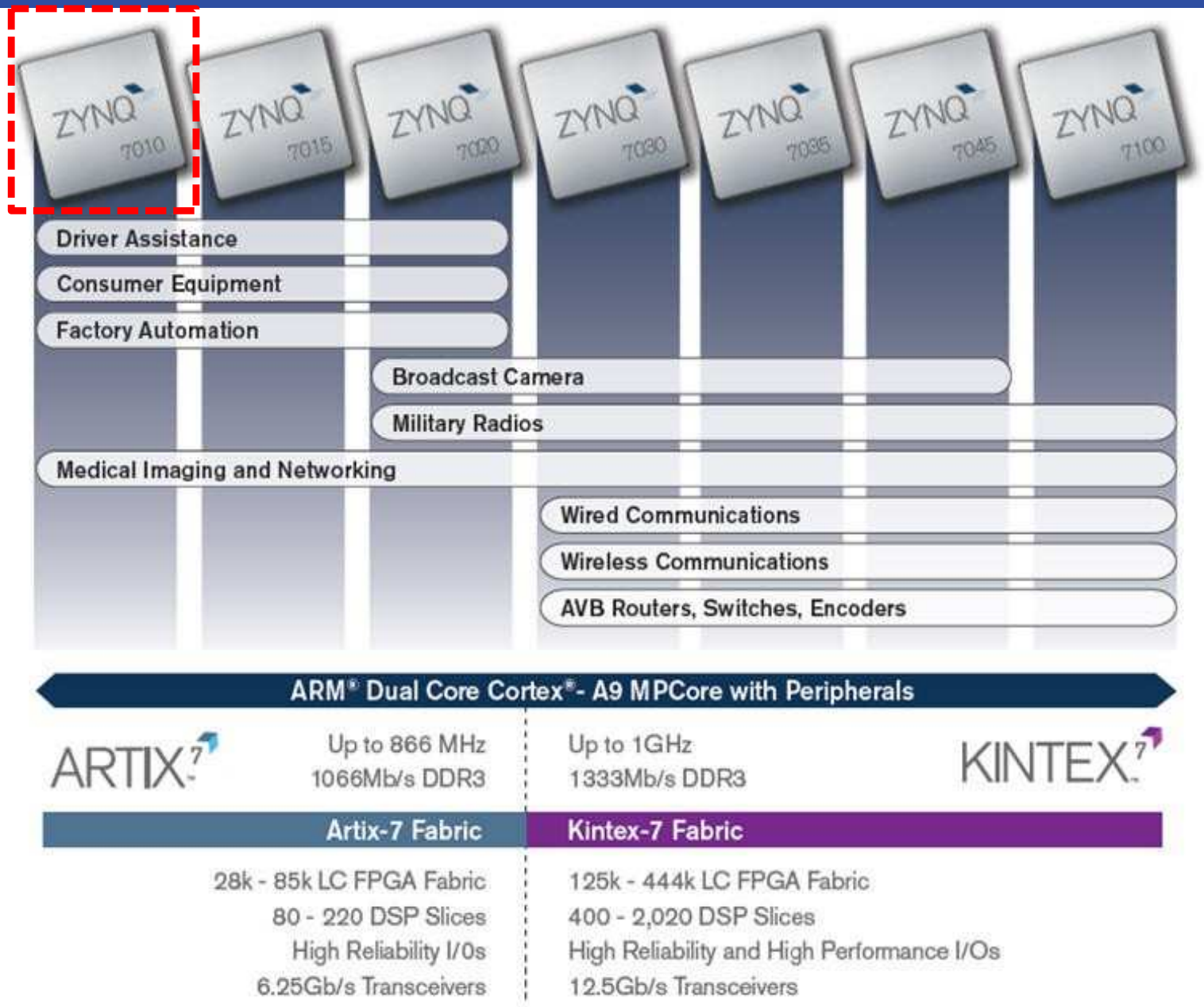
BEFEKTETÉS A JÖVŐBE

References

- AMD-XILINX official site
  📖 https://www.amd.com
- Xilinx Zynq data sheets
  📖 ds190.pdf – Zynq-7000-Overview
- Zynq-7000 Technical Reference Manual (UG-585) – 1800 pages!
  📖 https://docs.xilinx.com/r/en-US/ug585-zynq-7000-SoC-TRM



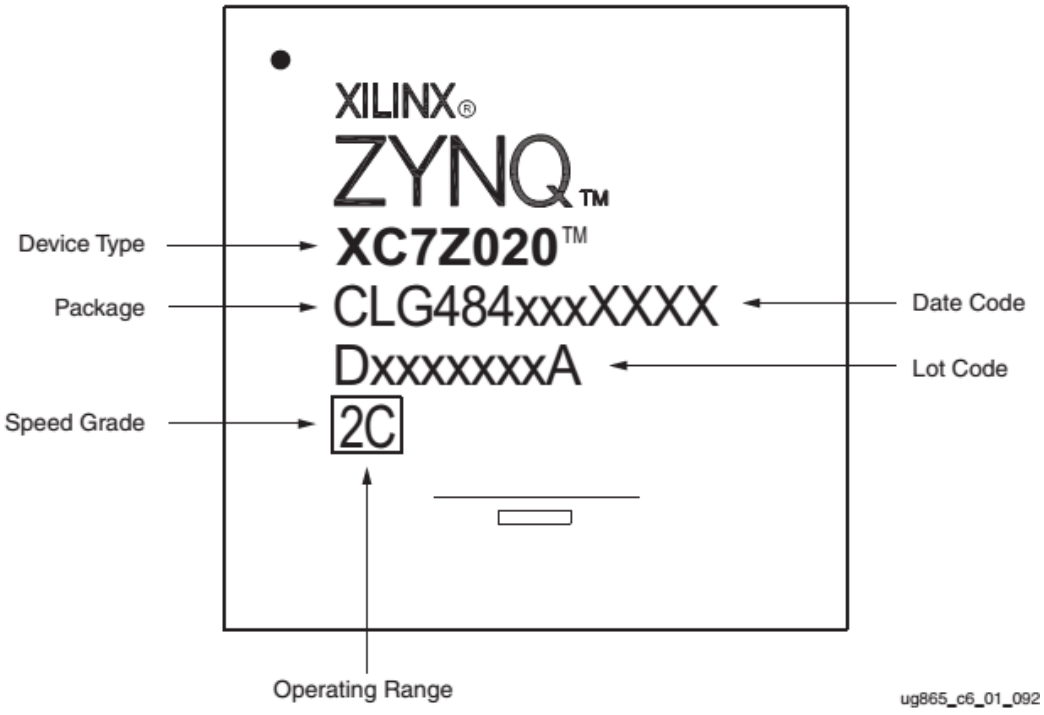
Zynq-7000 series



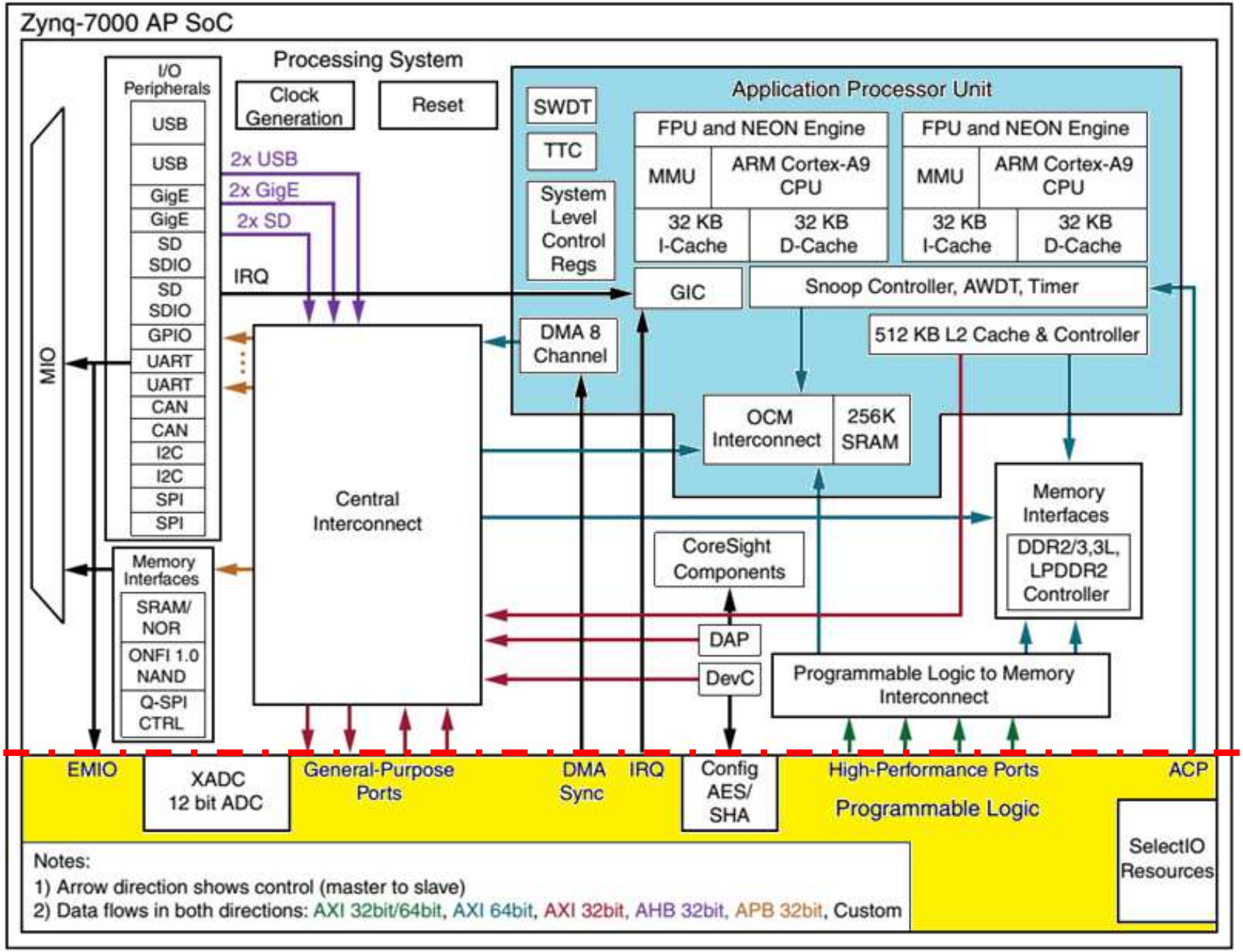
Choosing FPGA device - Catalogue

- Device type, Package, Pin Count
  - ZYNQ XC7Z010-1CLG400C* = Xilinx Zynq-7010 (~ 28.000 logic cells FPGA)
  - Chip Scale (CLG400C)
  - Pin Count: 400
  - Speed grade =**1**: (C - commercial: 0-85 C°)

* Valid for ZyBo platform



Xilinx Zynq APSoC = PS + PL



Processor System (PS)

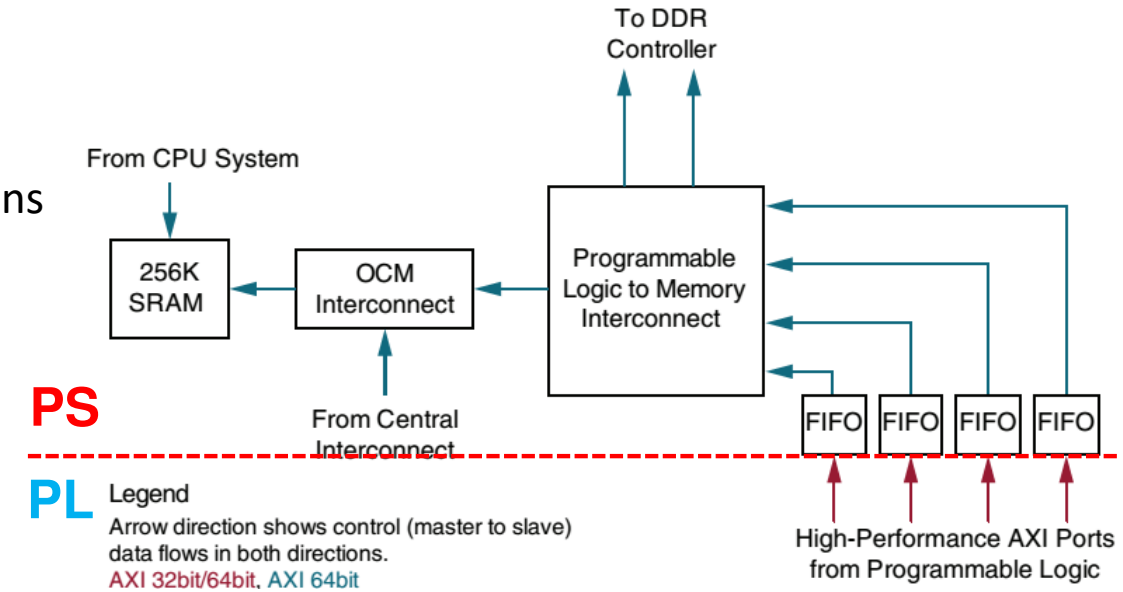
	Device Name	Z-7010	Z-7015	Z-7020
	Part Number	**XC7Z010**	**XC7Z015**	**XC7Z020**
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™		
	Processor Extensions	NEON™ & Single / Double Precision Floating Point		
	Maximum Frequency	667 MHz (-1); 766 MHz (-2); 866 MHz (-3)		
	L1 Cache	32 KB Instruction, 32 KB Data per processor		
	L2 Cache	512 KB		
	On-Chip Memory	256 KB		
	External Memory Support(1)	DDR3, DDR3L, DDR2, LPDDR2		
	External Static Memory Support(1)	2x Quad-SPI, NAND, NOR		
	DMA Channels	8 (4 dedicated to Programmable Logic)		
	Peripherals(1)	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Peripherals w/ built-in DMA(1)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD		
	Security(2)	RSA Authentication, and AES and SHA 256-bit		
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)		2x AXI 32b Master 2x AXI 32-bit Slave 4x AXI 64-bit/32-bit Memory AXI 64-bit ACP 16 Interrupts		

Programmable Logic (PL)

	Device Name	Z-7010
	Part Number	**XC7Z010**
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates)(3)	28K Logic Cells (~430K)
	Look-Up Tables (LUTs)	17,600
	Flip-Flops	35,200
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)
	Programmable DSP Slices (18x25 MACCs)	80
	Peak DSP Performance (Symmetric FIR)	100 GMACs
	PCI Express® (Root Complex or Endpoint)	—
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs
	Security(2)	AES and SHA 256b for

PS-PL interconnections („bridges”)

- **AMBA AXI interface** for high speed primary data communication
  - 2 pieces of 32-bit AXI masters, 2 pieces of 32-bit AXI slaves
  - 4 configurable 32/64-bit buffered (FIFO) AXI slave interfaces (with OCM or DDR memory access)
  - 1 piece of 64-bit AXI slave (ACP) - CPU memory cache coherence (L1 $, L2 $)
- DMA and Interrupt Manager (GIC)
  - Processor "event" bus
  - PL peripheral interrupt -> GIC (in PS)
  - 4 pieces of DMA channels (PL -> PS)
- EMIO: External peripheral I/Os
  - PS-side peripherals can also share PL pins
- 4 pieces of PS ***Clock*** outputs,
- 4 pieces of PS ***Reset*** signals to PL
- Configuration
  - **JTAG**
  - XADC
  - Processor Configuration Access Port (PCAP)



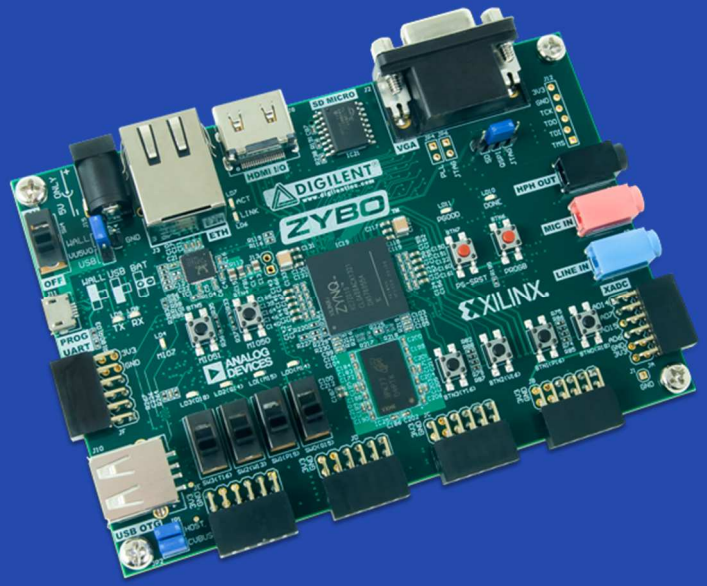
PL ~ FPGA fabric (Zynq 7010)

Zynq-7010 architecture based on the **Xilinx Artix-7** FPGA family !

- **CLB (inlcudes slices)**:
  - 8 pieces of LUT-6 / CLB: configurable logic block or distributed memory
    - LUT as „memory”: 64x1 bit RAM, or 32x2-bit RAM, or SRL – shift register
  - 16 pieces of FFs / CLB
  - 2x4-bit cascadable full adder (pl. FA)
- **BRAM** (36 Kbit):
  - Dual-port, max. 72-bits wide, or dual 18Kb BRAM memory
  - programmable dedicated FIFO
  - ECC support (72-bits Hamming coded data)
- **DSP** multiplier: (signed – 2’s complement, 25x18-bits)
  - 48-bit adder/accumulator
- Programmable **IOBs**: various standars (1.2-3.3V)
- Clock management: **PLL/MMCM** – 2-2 pieces
- **XADC**: 2 pieces of 12-bits A/D converter, 1 MSPS
  - on-chip voltage and temperature measurement, 17 differential input channel
  - https://docs.xilinx.com/r/en-US/ug480_7Series_XADC/7-Series-FPGAs-and-Zynq-7000-SoC-XADC-Dual-12-Bit-1-MSPS-Analog-to-Digital-Converter-User-Guide-UG480

DIGILENT ZYBO (ZYNQ BOARD)

Brief introduction of used development platform (HW)



SZÉCHENYI 2020

MAGYARORSZÁG KORMÁNYA

Európai Unió
Európai Strukturális és Beruházási Alapok

BEFEKTETÉS A JÖVŐBE

References

- 📖 ZYBO FPGA platform – official website:

www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,1198&Prod=ZYBO

- 📖 ZYBO Reference Manual (pdf):

www.digilentinc.com/Data/Products/ZYBO/ZYBO_RM_B_V6.pdf

- 📖 ZYBO Reference Manual (online):

https://reference.digilentinc.com/reference/programmable-logic/zybo/start

- 📖 ZYBO Schematic and PCB layout:

http://www.digilentinc.com/Data/Products/ZYBO/ZYBO_sch_B_V2.pdf

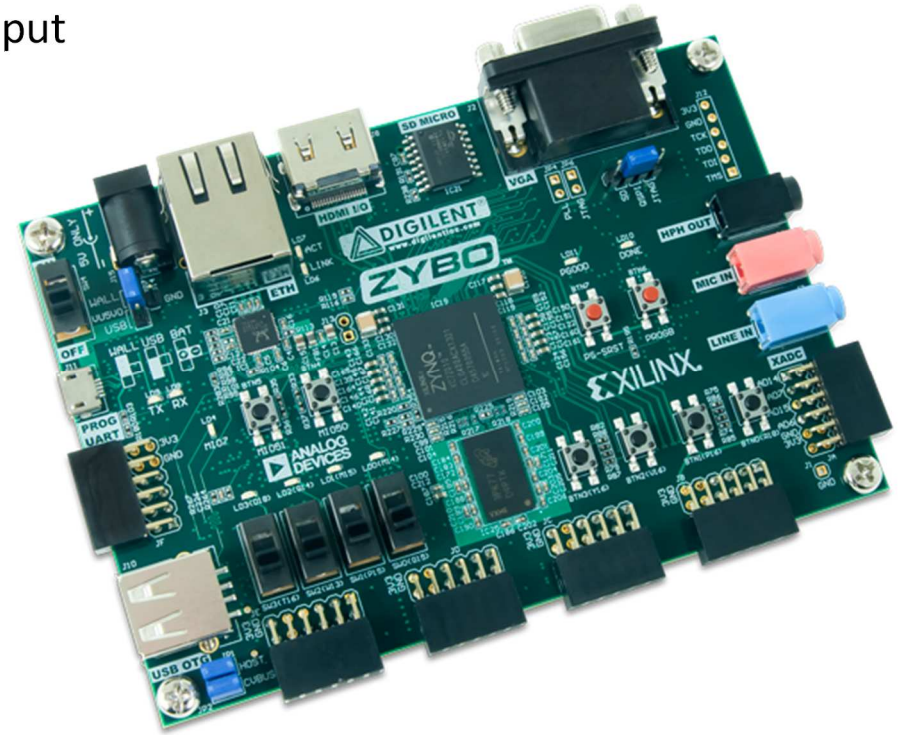
- 📖 The ZYNQ book (available after registration):

http://www.zynqbook.com/

Digilent ZyBo development platform

ZYBO™ Zynq FPGA/APSoC development kit

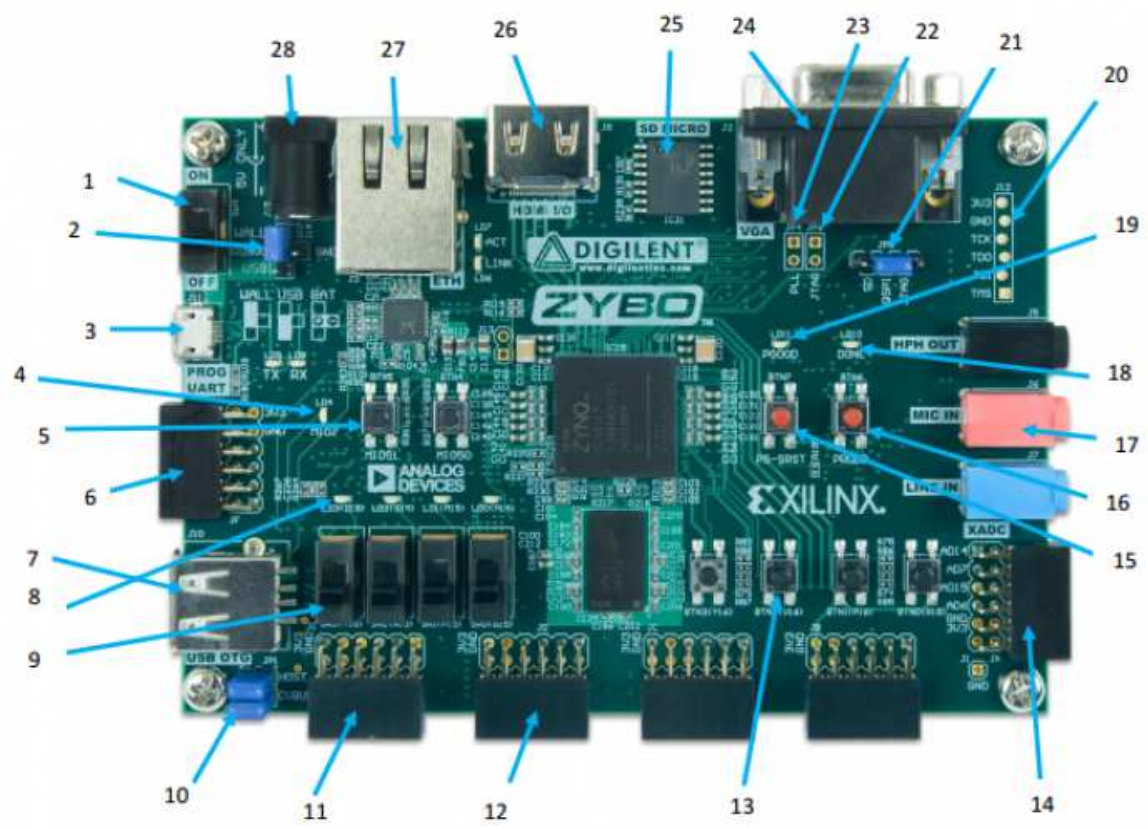
- *Xilinx Zynq-7000 (Z-7010)*
  - 650 MHz dual ARM Cortex-A9 cores (PS)
  - 8-channel DMA controller (PS)
  - 1G Ethernet, I2C, SPI, USB-OTG controller (PS)
  - Artix-7 FPGA logic (PL)
  - 28K logic cell, 240 Kbyte BRAM, 80 DSP multiplier (PL)
  - 12-bits, 1MSPS XADC (PL)
- 512 Mbyte DDR3 x32-bit (databus), 1050Mbps throughput
- Tri-mode 10/100/1000 Ethernet PHY
- HDMI port: Dual role (source/sink)
- VGA port: 16-bit
- uSD card: storing OS file system
- OTG USB 2.0 (host and device)
- Audio codec
- 128Mbit x Serial Flash/QSPI (storing configuration)
- JTAG-USB programmability, UART-USB controller
- GPIO: 4+1 LED, 4+2 push buttons, 4 dip switches
- 4+2 PMOD connector (+A/D)



📖 Webpage: https://store.digilentinc.com/zybo-zynq-7000-arm-fpga-soc-trainer-board/

Digilent ZyBo - Components

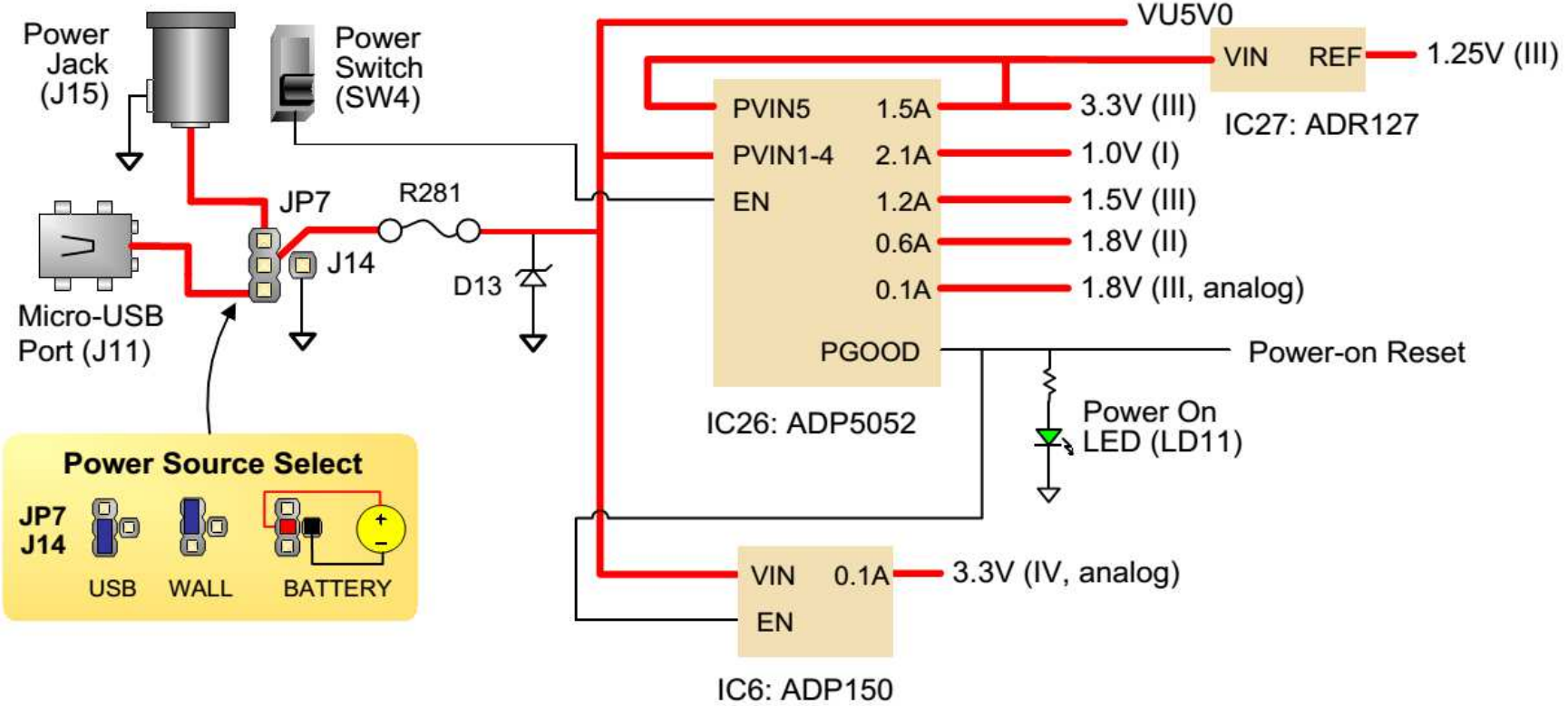
#	Component Description	#	Component Description
1	Power Switch	15	ARM Processor Reset Pushbutton
2	Power Select Jumper and battery header	16	FPGA Logic configuration reset Pushbutton
3	Shared UART/JTAG USB port	17	Audio Codec Connectors
4	MIO LED	18	Logic Configuration Done LED
5	MIO Pushbuttons (2)	19	Board Power LED
6	MIO Pmod	20	JTAG Port for optional external cable
7	USB OTG Connectors	21	Programming Mode Jumper
8	Logic LEDs (4)	22	Independent JTAG Mode Enable Jumper
9	Logic Slide switches (4)	23	PLL Bypass Jumper
10	USB OTG Host/Device Select Jumpers	24	VGA connector
11	Standard Pmod	25	microSD connector (Reverse side)
12	High-speed Pmods (3)	26	HDMI Sink/Source Connector
13	Logic Pushbuttons (4)	27	Ethernet RJ45 Connector
14	XADC Pmod	28	Power Jack



Power Supply

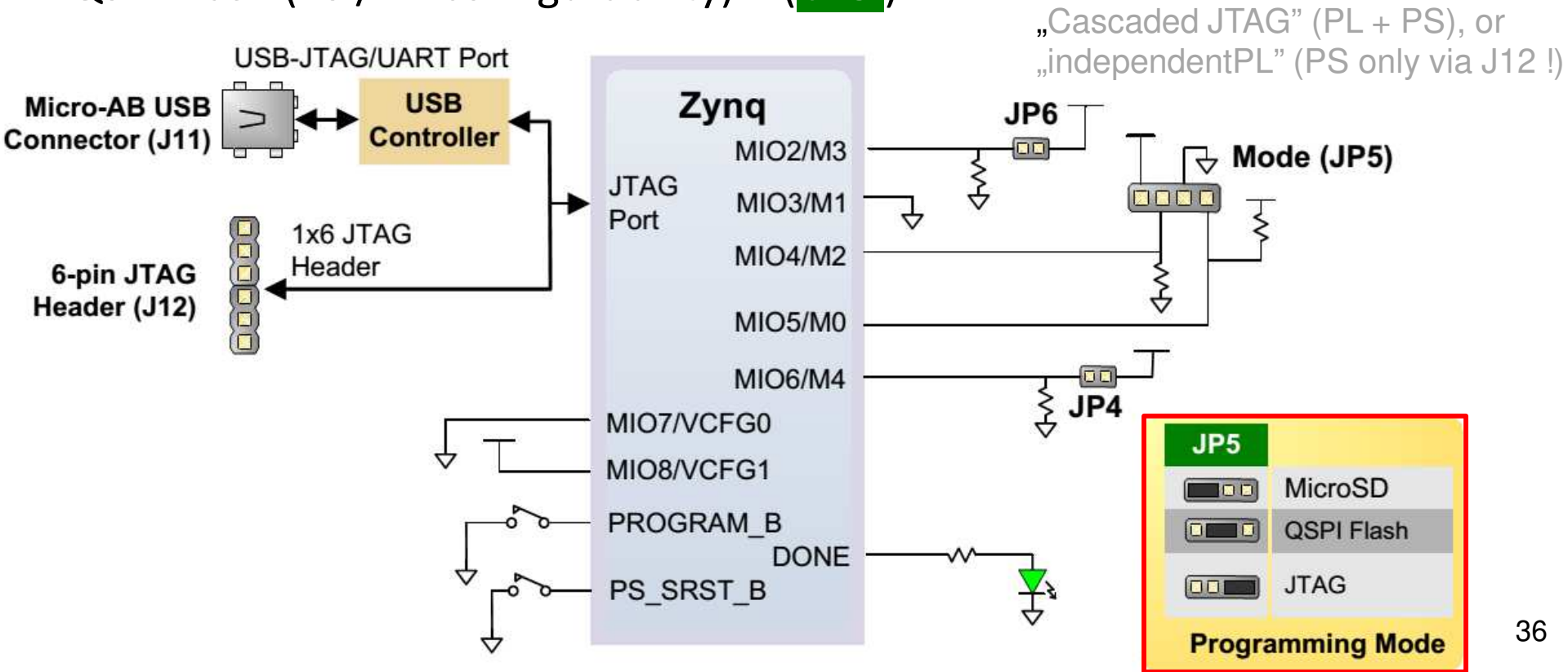
Three possible ways:

- **micro USB cable (max 0.5A),**
- wall connector: AC adapter 5V / 2.5A (Linux boot),
- battery.



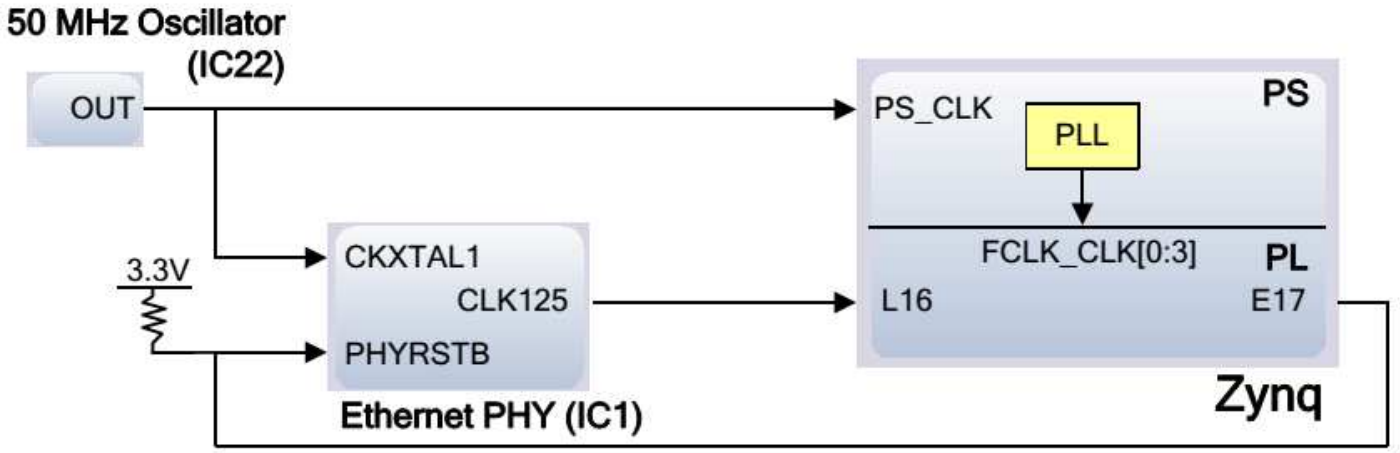
Configurability options

1. USB JTAG / UART interface (**J11**) it is the default,
2. JTAG (+ **debug** function J12 - not mounted): requires a special Xilinx Platform USB programming device (additional cost!),
3. MicroSD card (J4): e.g. Linux boot image (there are 3 phases of booting **BootRom → FSBL → SSBL** / SW Application), see LAB 11.
4. QSPI Flash (PS / PL configurability) - (**JP5**)



Clock sources

- 50 MHz PS_CLK (PS subsystem): 4 different reference clocks can be generated with PLL
- 125 MHz ref.clk (PL subsystem): independent from PS („L16” pin)
- ARM: max. 650 MHz clock (ARM PS PLL)
- DDR3 Memory controller: max. 525 MHz (1050 Mbps)



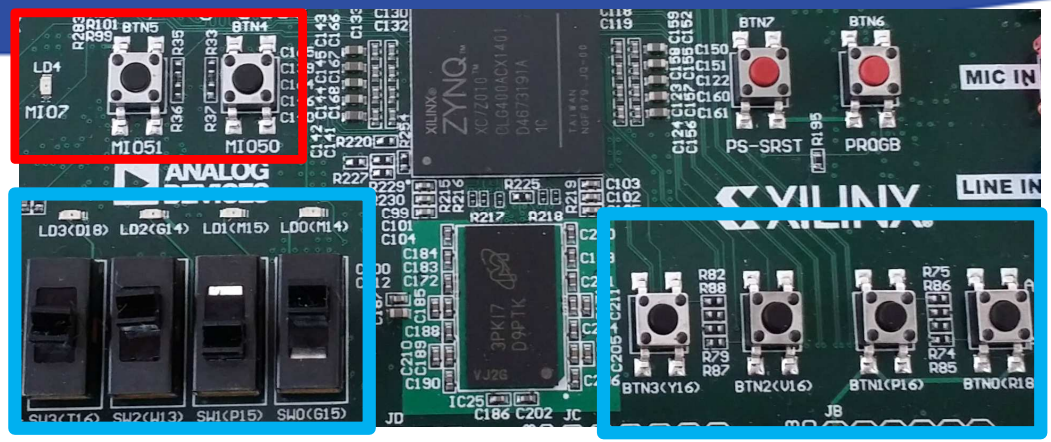
Programmable GPIO peripherals

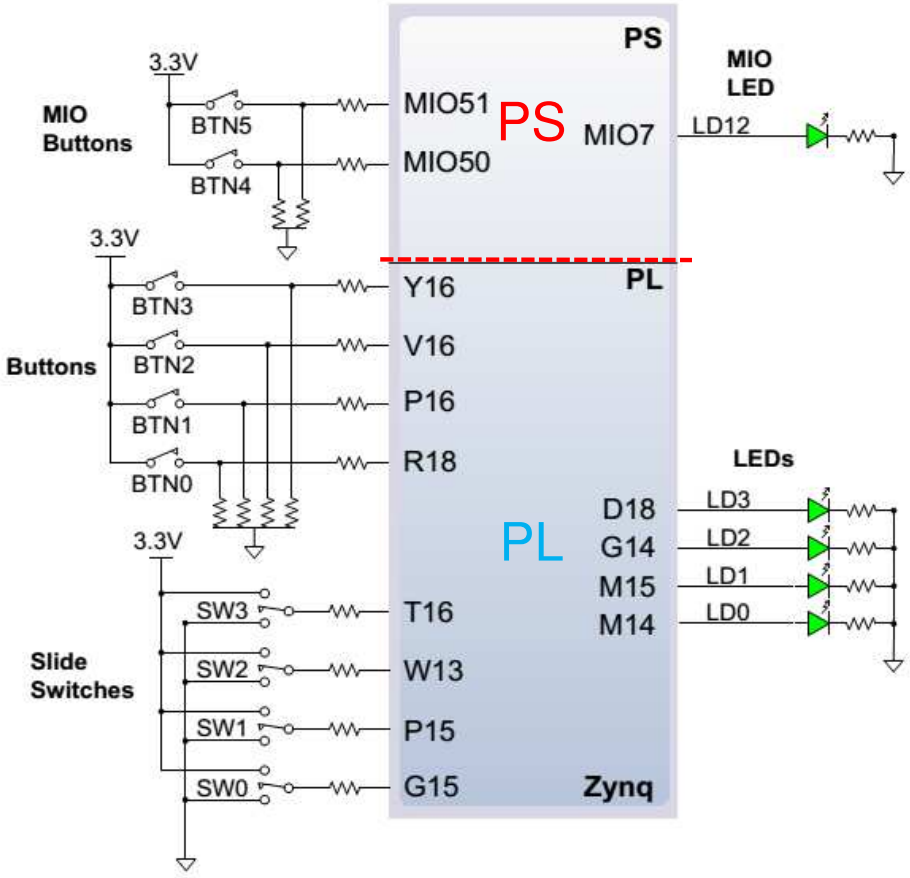
PS subsystem:

- Push buttons: 2
- LED: 1

PL subsystem:

- Push buttons: 4
- DIP switches: 4
- LEDs: 4





Push buttons:
'0': inactive
'1': active

DIP switches:
'0': inactive
'1': active

LED: (common cathod)
'0': inactive
'1': active

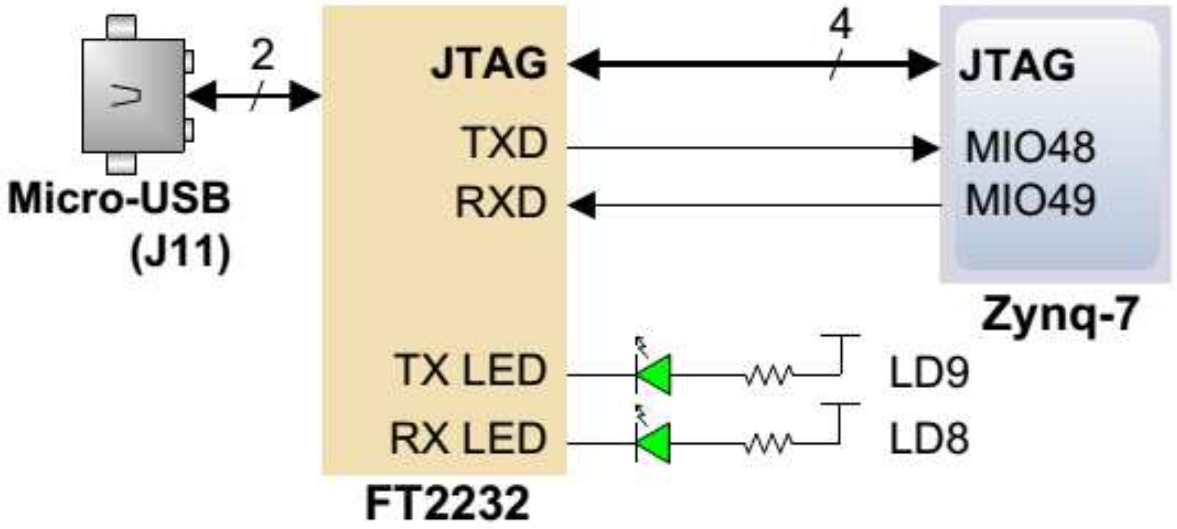
External memories

- Micron **DDR3** SDDRAM (**512 MByte**): *MT41K128M16JT-125 DDR3 memory*
  - Speeds up to max. 533 MHz -> 1066 Mbps (controller limited)
  - 32-bits data bus
  - PS (ARM) side dedicated memory with (hard-memory) controller

- Spansion serial **SPI Flash** 128Mbit (=**16 MByte**): *S25FL128S*
  - 1x, 2x SPI-, **4x QSPI** modes
  - Speeds up to max. 104 MHz, this translates to 400 Mbit/s (QSPI mode)
  - Both PS and PL side configurability

USB UART Bridge

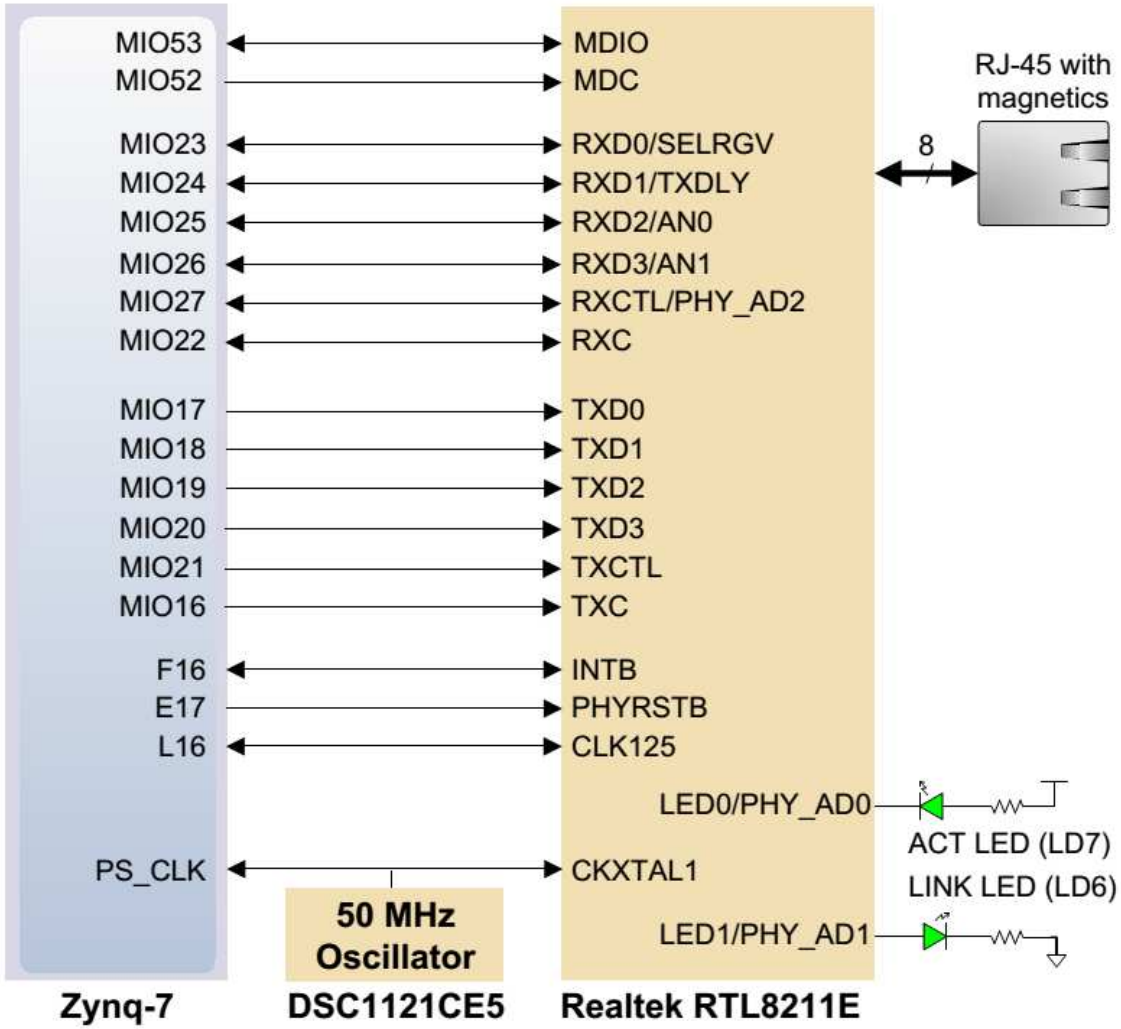
- FTDI USB-UART bridge (J11): *FT2232HQ*
  - USB <-> serial UART packet control,
  - Protocol settings: 115.200 baud rate, 1 stop bit, no parity, 8–bit data (char length),
  - Only PS side: MIO 48-49,
  - 2 in 1 functionality: JTAG-UART + power supply!



📖 FTDI: https://ftdichip.com/wp-content/uploads/2020/07/DS_FT2232H.pdf

Ethernet controller

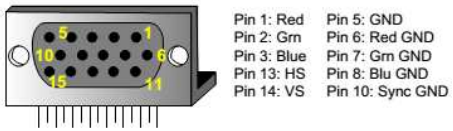
- Realtek RTL8211E-VL PHY : 10/100/1000 Mbit/s
  - RGMII transfer mode, Gigabit Ethernet MAC

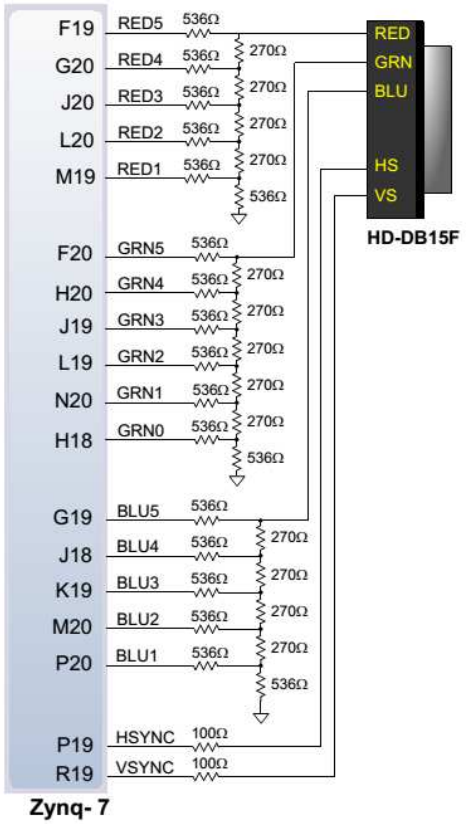


Video I/O

- VGA: 1 output port (16-bits of color depth: 5 Red, 6 Green, 5 Blue channels + HS, VS synchronization signals)
- HDMI: 1 input OR 1 output port (optional direction)

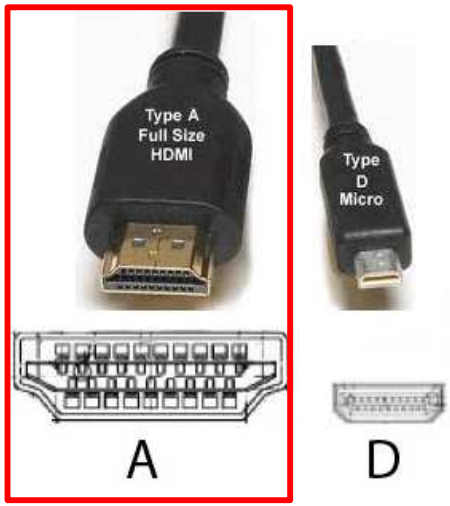
VGA





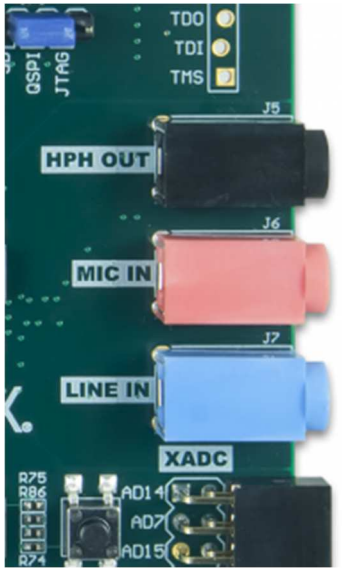
HDMI

- Configurable as Input, or ouptut HDMI port (PL)
  - ✓ Source / Sink mode
  - ✓ HDMI-A connector
- Support HDMI/DVI signals but there is no dedicated video codec chip on the PCB (implemented as FPGA logic)!



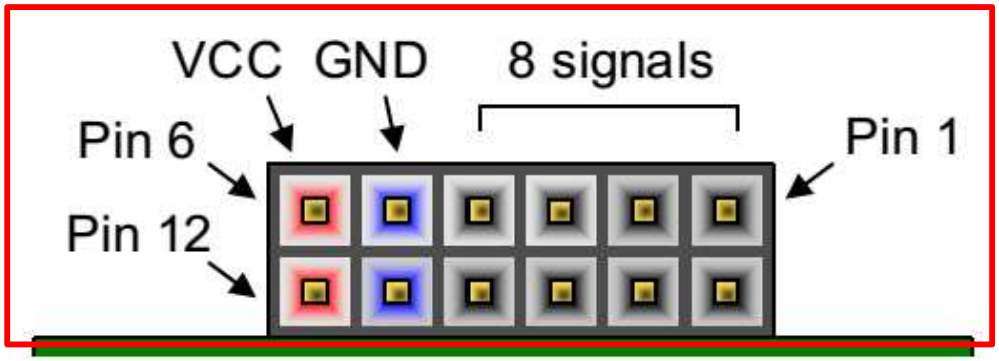
Audio

- Analog Devices SSM2603 audio codec
  - 8 - 96 KHz sampling rate,
  - mono microphone input,
  - stereo line-in input,
  - stereo output (3.5 mm jack).
- Connected to the PS-side via I²C bus interface
  - Audio data is transferred via the I²S protocol.



PMOD – Peripheral MODules

- 6 pieces of PMOD connectors
  - 12 pins = 2 power + 2 GND + 8 logic signals
  - Standard PMOD: accessed by PL side (4)
  - MIO PMOD: accessed by PS subsystem (1)
  - Dual **A/D** (XADC*) PMOD: **accessed by PL side** (1)
    - 12–bits A/D converter, 1 MSPS



* 📖 https://docs.xilinx.com/r/en-US/ug480_7Series_XADC/7-Series-FPGAs-and-Zynq-7000-SoC-XADC-Dual-12-Bit-1-MSPS-Analog-to-Digital-Converter-User-Guide-UG480

EFOP-3.4.3-16-2016-00009

A felsőfokú oktatás minőségének és hozzáférhetőségének együttes javítása a Pannon Egyetemen

THANK YOU FOR YOUR KIND ATTENTION!

SZÉCHENYI 2020

MAGYARORSZÁG KORMÁNYA

Európai Unió
Európai Strukturális és Beruházási Alapok

BEFEKTETÉS A JÖVŐBE