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APPENDIX A

Character Codes

ASCII Code

The following code was adopted as the American Standard Code for Information Interchange.

Table of ASCII Code Combinations
Format: HEX Representation of Bit Pattern, ASCII Coded Character

H	*E*	*H*	*E*	*H*	*E*	*H*	*E*	*H*	*E*	*H*	*E*	*H*	*E*	*H*	*E*
00	NUL	01	SOH	02	STX	03	ETX	04	EOT	05	ENQ	06	ACK	07	BEL
08	BS	09	HT	0A	LF	0B	VT	0C	FF	0D	CR	0E	SO	0F	SI
10	DLE	11	DC1	12	DC2	13	DC3	14	DC4	15	NAK	16	SYN	17	ETB
18	CAN	19	EM	1A	SUB	1B	ESC	1C	FS	1D	GS	1E	RS	1F	US
20	SP	21	!	22	"	23	#	24	$	25	%	26	&	27	'
28	(	29	)	2A	*	2B	+	2C	,	2D	–	2E	.	2F	/
30	0	31	1	32	2	33	3	34	4	35	5	36	6	37	7
38	8	39	9	3A	:	3B	;	3C	<	3D	=	3E	>	3F	?
40	@	41	A	42	B	43	C	44	D	45	E	46	F	47	G
48	H	49	I	4A	J	4B	K	4C	L	4D	M	4E	N	4F	O
50	P	51	Q	52	R	53	S	54	T	55	U	56	V	57	W
58	X	59	Y	5A	Z	5B	[	5C	\	5D	]	5E	^	5F	_
60	`	61	a	62	b	63	c	64	d	65	e	66	f	67	g
68	h	69	i	6A	j	6B	k	6C	l	6D	m	6E	n	6F	o
70	p	71	q	72	r	73	s	74	t	75	u	76	v	77	w
78	x	79	y	7A	z	7B	{	7C	|	7D	}	7E	~	7F	DEL

lines. The remaining portion of the logic in Figure B.31 is the refresh row counter. This counter is configured to count up by one each time the clock line is asserted (REFRESH-L). Thus, each time a refresh occurs, the row counter increments to point to the next row that needs to be refreshed. The memory modules used in this design are capable of refreshing two rows simultaneously, so the least significant address line of RC_BUS(8:0)-H is not involved in the count, and is driven low each time the refresh occurs.

The controller for the memory system is shown in Figure B.32. Dynamic RAM controllers are commercially available, so the system shown in the figure could be considered a "homemade" version of a RAM controller. The address is available when the ADS-L signal is asserted. Assertion of ADS-L sets a flag used by the controller (MEM_REQ_FLG-H), as well as identifying the direction of the transfer (with OUT-H). The controller itself is a state machine controller made with an 82S105 programmable device. This contains the logic and the register needed to control the memory system. The only requirement is to synchronize the inputs with the state machine, which is done by the '175 register. The controller asserts the signals needed (DO_RAS-H, DO_CAS-H, etc.) in the order needed to perform the work. Even though they work on the same principle, different dynamic RAMs have different timing requirements, and the system controller must be configured to meet the timing requirements of the modules being used. One of the characteristics of a dynamic RAM is the time permitted between refresh cycles. The 84300 shown in the figure is a refresh timer, and the input lines are configured to create a flag whenever a refresh cycle is needed to maintain the contents of the memory system. When the refresh request is satisfied, the flag is reset. The refresh takes priority over normal memory requests, so a system using a dynamic RAM memory must be capable of waiting for the results, since the memory request could occur when a refresh is in progress. Also included in the figure are the gates used to buffer the write enable lines. Since each write enable is connected to eight SIP modules, the drivers must be capable of handling the load of 72 individual devices. Finally, the transceivers that provide buffering for the individual bytes of the memory are separately enabled, and the gates that enable the transceivers are shown at the bottom of the drawing.

APPENDIX C

ICs Used in the Text

IC	*Description*
'00	Two input NAND gate
'02	Two input NOR gate
'04	Inverter
'05	Inverter — open collector output
'07	Inverter — open collector output, high voltage
'08	Two input AND gate
'10	Three input NAND gate
'20	Four input NAND gate
'30	Eight input NAND gate
'32	Two input OR gate
'74	Edge triggered D flip-flop
'86	Two input exclusive-OR gate
'125	Tri-state driver with low true enable
'133	Thirteen input NAND gate
'138	3-line-to-8-line decoder Inputs: 3 enables: 2 asserted low and 1 asserted high; 3 data inputs, asserted high Outputs: 8, asserted low
'139	2-line-to-4-line decoder Inputs: 2 data inputs, asserted high Outputs: 4, asserted low
'148	8-line-to-3-line priority encoder Inputs: 8 data lines, 1 enable line, all asserted low Outputs: 3 data outputs, 2 enable outputs, asserted low

IC	Description
'151	1-of-8 data selector/multiplexer: Inputs: 8 data, 3 select, asserted high; 1 enable, asserted low Outputs: high and low asserted data
'156	2-line-to-4-line decoder with open collector outputs Inputs: 2 data, asserted high; 2 enables, asserted low Outputs: 4, asserted low, open collector
'157	Quad 2-line-to-1-line data selector/multiplexer Inputs: 8 data lines, 1 select line, asserted high; 1 enable line, asserted low Outputs: 4 data lines, asserted high
'161	Synchronous 4-bit binary counter with direct clear Inputs: 4 data, 2 enables, one clock, asserted high; clear, load, asserted low Outputs: 4 data, 1 ripple carry out, asserted high
'164	8-Bit parallel out serial shift register Inputs: 2 data, 1 clock, asserted high; clear, asserted low Outputs: 8 data, asserted high
'165	8-Bit parallel in serial shift register Inputs: 8 data lines, serial in, clock, clock inhibit, asserted high load line, asserted low Outputs: 1 data line asserted both high and low
'174	6-Bit D-type register Inputs: 6 data, clock, asserted high; clear, asserted low Outputs: 6 data, asserted high
'175	4-Bit D-type register Inputs: 4 data, clock, asserted high; clear, asserted low Outputs: 4 data, asserted both high and low
'181	4-bit arithmetic logic unit/function generator Inputs: 8 data (2 4-bit data words), carry in, mode, 4 select lines, asserted high Outputs: 4 data (1 4-bit word), carry out, A=B out, asserted high, generate and propagate, asserted low
'182	Look-ahead carry generator Inputs: Generate and Propagate from 4 units, asserted low Outputs: 3 carry out lines, asserted high, generate and propagate, asserted low
'191	4-bit binary synchronous up/down counter Inputs: 4 data, clock, asserted high; load, count up, count enable, asserted low Outputs: 4 data, min/max, asserted high; ripple carry out, asserted low
'192	4-bit BCD up/down counter with dual clock Inputs: 4 data lines, two clocks, clear, asserted high; load, asserted low Outputs: 4 data lines, asserted high; two clocks, asserted low
'195	4-bit parallel access shift register Inputs: 4 data, J (for serial in), clock, asserted high; load, clear, K bar, (for serial in) asserted low Outputs: 4 data asserted high; one data asserted low

IC	Description
'198	8-bit bidirectional shift register Inputs: 8 data lines, left serial in, right serial in, two select lines, clock, asserted high; clear line, asserted low Outputs: 8 data lines, asserted high
'244	8-bit noninverting tri-state driver Inputs: 8 data, asserted high; two enable, asserted low Outputs: 8 data, asserted high
'245	8-bit noninverting tri-state bus transceiver Inputs: direction, asserted high; enable, asserted low I/O: two sets of 8 lines (bi-directional), asserted high
'260	5 Input NOR gate
'273	8-bit D-type flip-flop Inputs: 8 data lines, clock line, asserted high; clear line, asserted low Outputs: 8 data lines, asserted high
'283	4-bit binary adder Inputs: 8 data lines (2 4-bit words), carry in, asserted high Outputs: 4 data lines, carry out, asserted high
'286	9-bit parity generator/checker Inputs: 9 data lines, asserted high; transmit, asserted low Outputs: parity error, asserted low I/O: parity (generated or tested)
'299	8-bit bidirectional shift register with tri-state I/O Inputs: 2 select lines, right serial in, left serial in, clock, asserted high; clear, 2 enables, asserted low Outputs: two data outs (for serial shift), asserted high I/O: 8 data lines
'373	8-bit latch with tri-state outputs Inputs: 8 data lines, enable line, asserted high; output enable, asserted low Outputs: 8 data lines, tri-state
'374	8-bit register with tri-state outputs Inputs: 8 data lines, clock line, asserted high; output enable, asserted low Outputs: 8 data lines, tri-state
'520	8-bit identity comparator (2 8-bit words) Inputs: 16 data lines (2 8-bit words),asserted high; enable line, asserted low Outputs: equal, asserted low
'538	3-line-to-8-line decoder/demultiplexer with tri-state outputs Inputs: 3 data lines, output level select, 2 enable lines, asserted high; 2 enable lines, 2 output enables, asserted low Outputs: 8 data lines, asserted high or low
'540	8-bit tri-state driver with inverted outputs Inputs: 8 data lines, asserted high; 2 enables, asserted low Outputs: 8 data lines, asserted low
'541	8-bit tri-state driver Inputs: 8 data lines, asserted high; 2 enables, asserted low Outputs: 8 data lines, asserted high

IC	Description
'550	8-bit registered transceiver Inputs: 2 clocks, 2 flag clear lines, asserted high; 2 clock enables, 2 output enables, asserted low Outputs: two flags, asserted high I/O: 16 data lines (2 8-bit bidirectional groups)
'564	8-bit D registers with inverted tri-state outputs Inputs: 8 data lines, clock, asserted high; output enable, asserted low Outputs: 8 data lines, asserted low
'574	8-bit register with tri-state outputs Inputs: 8 data lines, clock line, asserted high; output enable, asserted low Outputs: 8 data lines, tri-state
'612	Memory mapper Inputs: 4 address lines, 4 register select lines, asserted high; chip select, map enable, map mode, write, asserted low Outputs: 12 data lines, asserted high I/O: 12 data lines, bidirectional
'620	8-bit noninverting tri-state bus transceiver Inputs: enable, asserted high; enable, asserted low I/O: two sets of 8 lines (bi-directional), asserted high
'645	8-bit noninverting tri-state bus transceiver Inputs: direction, asserted high; enable, asserted low I/O: two sets of 8 lines (bi-directional), asserted high
'646	8-bit bus transceiver and registers with tri-state outputs Inputs: 2 clocks, 2 source lines, direction, asserted high; enable, asserted low I/O: 16 lines (2 8-bit words, bidirectional)
'763	8-bit buffer with open collector outputs Inputs: 8 data lines, asserted high; 2 enables, asserted low Outputs: 8 data lines, asserted low (open collector)
'804	Two input NAND with high current capability
'843	9-bit register with tri-state output Inputs: 9 data lines, clock, asserted high; output enable, preset, clear, asserted low Outputs: 9 data lines (tri-state outputs)
'857	6-bit 2-line-to-1-line multiplexer Inputs: 12 data (2 6-bit words), 2 select, output polarity select, asserted high Outputs: 6 data (tri-state, polarity determined by input), input equal to zero, asserted high
'867	8-bit synchronous up/down counter Inputs: 8 data lines, clock, 2 select lines, asserted high; 2 enables, asserted low Outputs: 8 data lines, asserted high; ripple carry out, asserted low
'869	8-bit synchronous up/down counter Inputs: 8 data lines, clock, 2 select lines, asserted high; 2 enables, asserted low Outputs: 8 data lines, asserted high; ripple carry out, asserted low
'881	4-bit ALU, similar to '181

IC	Description
'882	32-bit look-ahead carry generator Inputs: generate, propagate from 8 stages, asserted low; carry in, asserted high Outputs: 4 carry outs, asserted high
82S105	Field programmable sequencer
84244	8-Bit Non-Inverting Tri-State Driver, Trapazoidal Drive Inputs: 8 data, asserted high; two enable, asserted low Outputs: 8 data, asserted high
84300	Programmable refresh timer Inputs: 8 data lines, clock, asserted high; refresh, chip enable, chip enable, asserted low Outputs: 8 data lines, refresh request asserted low; refresh clock, asserted high
AM2901	4-bit microprocessor slice Inputs: 4 A address lines, 4 B address lines, 9 instruction lines, 4 data lines, carry in, clock, asserted high; output enable asserted low Outputs: 4 data lines, overflow, equal, sign, carry out, asserted high; propagate, generate, asserted low I/O: 4 shift lines
AM2910	Microprogram controller Inputs: 12 data lines, 4 instruction lines, carry in, clock, asserted high: output enable, condition code, condition code enable, register load, asserted low Outputs: 12 data lines, asserted high; map enable, PL enable, VEC enable, full, asserted low
IDT7423	16×16 Multiplier/accumulator
L16R8	Programmable logic array
27S45	Registered PROM

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